



Workshop

“CMOS detectors for high performance applications”

8 - 9 december 2009

Institut Aéronautique et Spatial
23 Avenue Edouard Belin, TOULOUSE

Co-organised by CNES, Astrium, THALES ALENIA SPACE

PROGRAMME

Over the past two decades dramatic improvements have been carried out to increase performance and capability of CMOS image sensors.

A wide range of architectures, technologies and features is now available to meet the continuously growing variety of applications ranging from cellular phones on the low end to high quality digital still photography or scientific applications on the high end.

CNES, Astrium and Thales Alenia Space are pleased to invite you to attend the « CMOS detectors for high performance applications » workshop to be held in Toulouse on December 8th – 9th, 2009 within the framework of the Optics and Optoelectronics Technical Expertise Center.

The aim of this workshop is to focus on the new generation of CMOS image sensors that are able to compete with CCD image sensors in the field of high quality imaging thanks to significant improvements in the following key parameters :

- noise
- sensitivity
- dynamic range
- MTF
- high speed

Topics

The workshop shall address all the axes investigated to improve CMOS detector performances :

- materials (thin film, optical layers, dopant, amorphous Si,...)
- processes (back-thinning, hybridization,...)
- optical and electrical design (micro-lenses, low noise amplifiers, shutter, CDS,...)
- large format (stitching, small pixel pitch...)
- operating conditions (TDI, low temperature,...)

Although the workshop is mostly oriented to visible/NIR spectral range, and considering the synergies existing between monolithic CMOS detectors and hybrid arrays (low noise/low flux read out, dynamic range improvement, large frame rate devices...), this event is fully open to teams working on high performances IR and UV CMOS detectors. Teams developing non-space applications addressing high performances are also welcome to participate to this workshop.

Oral presentation shall be requested for the workshop.

Round Table

The workshop will include a round table focused on the access to CIS processes for small volumes and high performance applications.

Workshop official language

The official language for the workshop is English.

Registration

Registration is free of charge. On-line registration <http://cnes.cborg.net/cct/bipublicgb.html>

Calendar

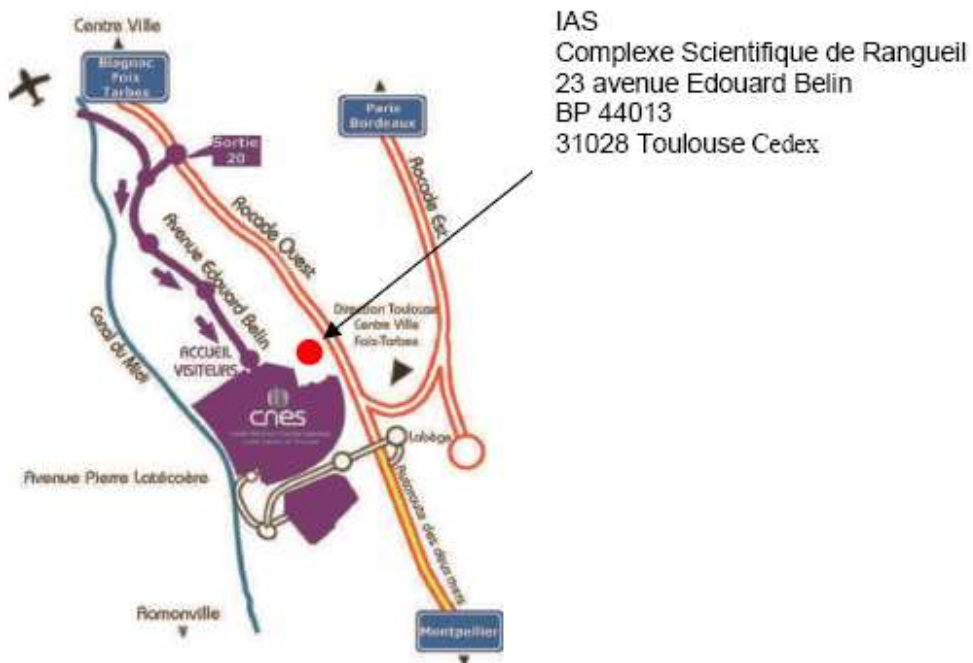
November 27th : deadline for registration
December 8th ; 9th : workshop

Organization committee

Alex MATERNE	CNES	alex.materne@cnes.fr	33.(0)5.61.28.15.44
Olivier SAINT-PE	Astrium	Olivier.Saintpe@astrium.eads.net	33.(0)5.62.19.67.16
Christophe RENARD	Thalès Alenia Space	Christophe.Renard@thalesalieniaspace.com	33.(0)4.92.92.70.08

Contact : alex.materne@cnes.fr

Workshop location :



Programme

December 8th. Morning session.

<i>Begin</i>	<i>Durat</i>	<i>speaker</i>	<i>Organism</i>	<i>Title</i>
10h00	10mn	Alain BARDOUX	CNES	Introduction
10h10	30mn	Emmanuel MOUTAYE	INPT ENSEEIH- LOSE	Avalanche photodiode in standard CMOS technology for high sensitivity embedded applications
10h40	30mn	B. DIERICKS	CAELESTE	Hybrid photon-counting and ranging Avalanche Photodiode array
11h10	30mn			BREAK
11h40	30mn	Boyd FOWLER	FAIRCHILD IMAGING	Low Noise High Dynamic Range CMOS Image Sensor for High Performance Imaging Applications
12h10	30mn	Thomas BAECHLER	CSEM	Single-Photon Resolution CMOS Integrating Image Sensors
12h40				LUNCH

December 8th. Afternoon session.

<i>Begin</i>	<i>Durat</i>	<i>speaker</i>	<i>Organism</i>	<i>Title</i>
14h00	15mn	Alex MATERNE	CNES	Requirements for CMOS imaging sensors for high resolution LEO observation satellites
14h15	25mn	Gerald LEPAGE	CMOSIS	Architectures for high resolution TDI CMOS sensors for LEO satellites
14h40	30mn	Patrick ROBERT	ULIS	High Dynamic Range in a VGA uncooled infrared focal plane arrays.
15h10	30mn	O. NIXON	DALSA	High Quality Video-Rate Imaging with 12 MegaPixel resolution
15h40	30mn			BREAK
16h10	30mn	Jerome PRATLONG	e2v technologies	Very high speed low noise CMOS sensor
16h40	30mn	Bart CREMERS	CYPRESS Semiconductor	A High Speed Pipelined Snapshot CMOS image sensor with 6.4 Gpixel/s data rate
17h10	20mn	Arnaud PEIZERAT	CEA- LETI	Analog to digital converter for image sensors
17h30	1h00	Assemblée générale du CCT OOE Annual General meeting of the CCT OOE		
18h30				COCKTAIL

December 9th. Morning session.

<i>Begin</i>	<i>Durat</i>	<i>Speaker</i>	<i>Organism</i>	<i>Title</i>
9h00	30mn	Ibrahima DJITE	ISAE	Modulation transfer function (MTF) and charge collection efficiency in CCD and CMOS image sensors: analysis and modelling
9h30	30mn	Stephane DEMIGUEL	SAGEM Défense Sécurité	High responsivity backside illuminated CMOS detectors for defense applications
10h00	30mn	Paul JERRAM	e2v technologies	Recent Results from Back-Thinned CMOS imagers
10h30	30mn	O. NIXON	DALSA	Backside Thinning Process for Large Sized Dies with High QE and Compatible with Low Temperature Operation
11h00	20mn			BREAK
11h20	1h10	Round table Access to CIS processes for small volumes and high performance applications		
12h30				LUNCH

December 9th. Afternoon session

<i>Begin</i>	<i>Durat</i>	<i>Speaker</i>	<i>Organism</i>	<i>Title</i>
14h00	30mn	Michel ZECRI	SOFRADIR	SOFRADIR recent developments in Infrared Imaging Sensors for Astronomy and Space applications
14h30	30mn	Michel BREART DE BOISANGER	EADS ASTRIUM	COBRA : CMOS space qualified detectors for space optical instruments
15h00	30mn	Ben DRYER	e2v centre for electronic imaging	Radiation Damage Study of 0.18 µm Process CMOS Image Sensors
15h30	20mn			BREAK
15h50	30mn	Cedric VIRMONTOIS	ISAE	Ionization and Displacement Damage on Deep Sub-Micron CMOS Image Sensors
16h20	/			End of the workshop

Round Table Outline

Access to CIS processes for small volumes and high performance applications

Under the high pressure of the consumer markets, most of the R&D efforts in CMOS image sensors (CIS) aim at shrinking the pixel size.

Pixels less than 2 μm are currently achieved thanks to a wide range of design and process improvements:

- very deep (sub 100 nm) processes,
- reduction of the thickness of the upper stack (dielectric and metal layers),
- optimization of the optical path thanks to micro-lenses, wafer thinning and backside illumination,
- use of n type and SOI substrates.

Beside this struggle for super small pixels, the world of high performance applications- including space applications - remains few steps backward with performance requirements that set the optimum pixel size in the range [5 – 15 μm] for a volume of products thousand times lower than requested for consumer applications.

Moreover, the little world of high performance applications does not have, most of the times, the necessary funding capacity to develop dedicated processes.

In such a context the safer rule is to deal with the existing and evolving processes and try to get the best of them for our applications.

The round table will start with a review of the main advances in processes for consumer applications, and will attempt for each innovative process to balance the advantages and drawbacks when transferred to larger pixels applications.

The recurrent questions that are shared by the small community of high end applications will be discussed:

- Will our applications follow the shrinking trend : where is the limit ?
- To which extent are the current processes still applicable to larger pixels?
- Which new processes are directly profitable for large pixels applications?
- What are the reliability impacts of processes dedicated at small pixels?
- What is the capability of simulation tools to transfer performance prediction from small to larger pixels?
- How to adapt to the fast evolution of CMOS processes and the continuous movement of foundries landscape? What could be the part of European institutions (EC, space, defence, research agencies....) in order to improve the access to CIS processes
- Is there a chance to see the emergence of advanced CIS foundries able to offer small volumes for high performance applications?