Coupling Test and Optical Techniques to improve functional logic failure localization

Dr. Aziz Machouat
STMicroelectronics Rousset (France)
Motivations

- Limits of current techniques used for functional logic failure localization:

ATPG Diagnostic

- Length of net : 500µm
- Length of net : 600µm

Optical techniques

- OBIRCh localization (1µ²)
- TEM lamella
- Failing contact

List of candidates

- Net 1
- Net 2
- Net 3
- Net 4
- ...
- Net 42

Alternatives techniques are needed
Agenda

1. Presentation of a methodology for improving accuracy of functional logic failure localization:

2. Correlation of static and dynamic optical techniques for the same defect in order to improve defect localization

3. Effect of physical defect on voltages-periods shmoos plots
1. Methodology for improving accuracy of functional logic failure localization

The implemented method combines ATPG diagnostic and optical techniques:

- The investigation area for the physical analysis is greatly reduced.

The implemented method combines ATPG diagnostic and optical techniques.
1. Description of the method in a case study

- ASIC in 130nm technology node, yield loss in « Scan stuck-at » test
- ATPG diagnostic:

```plaintext
#failing_pat=278, #failures=763, #defects=1, #faults=4, CPU_time=9.48
Simulated : #failing_pat=278, #passing_pat=900, #failures=763

Fault candidates for defect 1: stuck fault model, #faults=4, #failing_pat=278, #passing_pat=900

match=44.43%, #explained patterns: <failing=137, passing=795>
sa1 DS  s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/A (F_FA1LL)

match=41.06%, #explained patterns: <failing=127, passing=781>
sa0 DS  s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/A (F_FA1LL)

match=25.11%, #explained patterns: <failing=2, passing=822>
sa0 -- s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_3/CI (F_FA1LL)
sa0 -- s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/CO (F_FA1LL)

match=23.76%, #explained patterns: <failing=12, passing=754>
sa1 DS  s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_3/CI (F_FA1LL)
sa1 -- s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/CO (F_FA1LL)
```

6 faults
2 electrical nets

Localization of nets at layout level
1. Description of the method in a case study

- Localization by static optical technique OBIRCh:

- OBIRCh image
- Overlay between OBIRCh and circuitry images
1. Description of the method in a case study

Correlation between ATPG diagnostic and OBIRCh localization:

List of nets passing through the OBIRCh spot:

- Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/n883
- Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/Xr460/XU1_2/gnd
- Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/odd_phase[1]
- Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/Xr460/XU1_2/Cl
- Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/Xr460/XU1_2/A
- Xs850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_3/CI
- Xs850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/CO

List of nets proposed by the ATPG diagnostic:

- s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/A
- s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_3/Cl
- s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/CO

13 nets

Only 1 candidate after correlation
1. Description of the method in a case study

Effectiveness of the methodology:

<table>
<thead>
<tr>
<th>Layers to observe</th>
<th>Localization by ATPG diagnostic</th>
<th>OBIRCh localization</th>
<th>Localization by the methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>2</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>3</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>Contacts</td>
<td>7</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>Metal 1</td>
<td>6</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>Metal 2</td>
<td>6</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Metal 3</td>
<td>5</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>Metal 4</td>
<td>2</td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>Total</td>
<td>31</td>
<td>19</td>
<td>3</td>
</tr>
</tbody>
</table>

The methodology allows to focus the physical analysis only on 3 interconnection layers
1. Description of the method in a case study

- Physical analysis: Delayering, Cross-section & TEM

The short is due to residue of Titanium
2. Correlation of static and dynamic optical techniques

- On the same defect, we can use static and dynamic techniques based on test results.

- By doing so, localization can be improved by combining the two approaches.
2. Correlation of static and dynamic optical techniques

How to define test pattern for static and dynamic techniques:

Characterization of the functionality of the device for a failing test pattern

Tests for operating points P1 and P2 allow to define shmoo plot shape

\[ P1 = \frac{V_{dd \ max}}{Period \ max} \]
\[ P2 = \frac{V_{dd \ min}}{Period \ min} \]
2. Correlation of static and dynamic optical techniques

For the same defect, the test define:
- Failing test patterns for static analysis (P12, P15, ...)
- Failing test patterns for dynamic analysis (P1, P16)
2. Correlation of static and dynamic optical techniques

- New flow for functional failure localization:
  
  - Defect
  - Pattern A
    - Static localization techniques
  - Pattern B
    - Dynamic localization techniques
  - To combine the 2 approaches in order to improve localization
2. Case study: Correlation of static and dynamic optical techniques

- ASIC in 130nm technology node, yield loss in « Scan stuck-at » test

**Test conditions: Vdd max / period max**

- DATALOG 1
  - 39 "HVCTRL" 1555
  - 42 "HVCTRL" 1555
  - 47 "HVCTRL" 1555
  - 48 "HVCTRL" 1555
  - 54 "HVCTRL" 1555
  - 62 "HVCTRL" 1555
  - 67 "HVCTRL" 1555
  - 77 "HVCTRL" 1555
  - 78 "HVCTRL" 1555
  - 81 "HVCTRL" 1555

**Test conditions: Vdd min / period min**

- DATALOG 2
  - 39 "HVCTRL" 1555
  - 42 "HVCTRL" 1555
  - 44 "HVCTRL" 1555
  - 47 "HVCTRL" 1555
  - 48 "HVCTRL" 1555
  - 54 "HVCTRL" 1555
  - 59 "HVCTRL" 1555
  - 62 "HVCTRL" 1555
  - 67 "HVCTRL" 1555
  - 77 "HVCTRL" 1555
  - 78 "HVCTRL" 1555
  - 79 "HVCTRL" 1555

The defect is detected for the same flip-flop

The test patterns 44, 59 and 79 have a Pass/Fail border in the shmoo plot
2. Case study: Correlation of static and dynamic optical techniques

- Correlation of optical techniques:

  1. Defect

Pattern A
Static technique « OBIRCh »
- 3 area are located
- Where is the defect?

Pattern B
Dynamic technique « SDL »
- Only 1 area is located by « Soft Defect Localization » (SDL) technique. Localization and accuracy have been improved
1-2. Conclusion – Methodology for improving accuracy of functional logic failure localization

A methodology for improving functional logic failure localization have been presented. This methodology combines optical techniques and ATPG diagnostic.

In this methodology static and dynamic optical techniques can be used for the same defect based on test result.

This approach can be very useful to improve defect localization.
3. Effect of defect in periods-voltages

*shmoo plot*

- The study was performed using spice simulations
- The simulated structure is a 4 inverters chain
- Simulated defect: pull-up, pull-down, intra-cell bridge, serial resistance, open circuit

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**Shmoo plot of reference circuit**

*Optical Localization Techniques Workshop, Toulouse, January 27th, 2009*
3. Effect of « pull-up » defect type

- For $R < 1.25\,\text{KO}$, « hard defect »
- For $R > 5\,\text{KO}$, the defect does not affect the functionality of the circuit
- For $1.25\,\text{KO} < R > 5\,\text{KO}$, a pass/fail border is observed in the shmoo plot

A low variation of defect resistance causes a large variation in the shmoo plot
3. Conclusion - Effect of defect in periods-voltages shmoo plot

- **Bridge defect type**: A low variation of the defect resistance generates a high variation in shmoo plot. Statistically, the defect will not affect the functionality of the circuit or it can not be localized by dynamic optical techniques.

- **Resistive path defect type**: There is a pass/fail border for a wide range of defect resistances. So, dynamic techniques are more appropriate to this type of defect.

<table>
<thead>
<tr>
<th>Defect Type</th>
<th>Critical Value</th>
<th>Critical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull-up</td>
<td>&lt; 1.25 KO</td>
<td>&gt; 5 KO</td>
</tr>
<tr>
<td>Pull-down</td>
<td>&lt; 0.85 KO</td>
<td>&gt; 2 KO</td>
</tr>
<tr>
<td>Intra-cell bridge</td>
<td>&lt; 1.5 KO</td>
<td>&gt; 5 KO</td>
</tr>
<tr>
<td>Serial resistance</td>
<td>&gt; 60 KO</td>
<td>&lt; 5 KO</td>
</tr>
</tbody>
</table>

- « Bridge » defect type
- « Resistive path » defect type